Claims 1-25. (Canceled).

26. (Currently Amended) A process of forming a semiconductor structure, comprising:

forming a plurality of high and low density areas of nFETS and pFETs on a substrate, the high density areas exhibiting a gate to gate distance of 130 nanometers or less and the low density areas exhibiting a gate to gate distance of greater than 130 nanometers ~~or greater~~;

forming a thin compressive film of at least one of Si_xN_y and Si_xON_y in a range of 20 to 50 nanometers in channel regions of the high density areas of pFETs exhibiting a compressive stress of approximately -1400 MPa;

forming a thin tensile film of at least one of Si_xN_y and Si_xON_y in a range of 20 to 50 nanometers in channel regions of the high density areas of nFETs;

forming a thick compressive film of at least one of Si_xN_y and Si_xON_y in a range of 50 to 500 nanometers in channel regions of the low density areas of pFETs;

forming a thick tensile film of at least one of Si_xN_y, and Si_xON_y in a range of 50 to 500 nanometers in channel regions of the low density areas of nFETs exhibiting a tensile stress of approximately 700 Mpa,

wherein the forming of the thick tensile film includes providing:

a temperature of approximately 480°C, a pressure of approximately 6.25 Torr, a spacing between the substrate and electrode of 490 mils, and a flow of 300 sccm of 2% dilute SiH_4 gas, 15 sccm NH_3 gas and 1060 sccm N_2 gas using RF power of 340 watts, and

wherein the forming of the thin compressive film includes providing:

a temperature of approximately 480°C, a pressure of approximately 5.75 Torr, a spacing between the wafer and the electrode of 395 mils, and a flow of 3000 sccm of 2% dilute SiH_4 gas, 15 sccm NH_3 gas and 1060 sccm N_2 gas using RF power of 900 watts.

27. (New) The process of claim 26, wherein the 20 to 50 nanometer thickness of the thin compressive film does not pose a substantial risk of void formation.

28. (New) The process of claim 26, wherein the 20 to 50 nanometer thickness of the thin tensile film does not pose a substantial risk of void formation.

29. (New) The process of claim 26, wherein a compressive stress of the thin compressive film enhances performance of the high density areas without materially

degrading performance of the low density areas and a tensile stress of the thin tensile film enhances performance of the high density areas without materially degrading performance of the low density areas.

30. (New) The process of claim 26, wherein the thin compressive film and the thin tensile film are formed by one of a CVD process, a plasma enhanced CVD process and a PVD process.

31. (New) The process of claim 26, wherein the thick compressive film and the thick tensile film are formed by one of a CVD process, a plasma enhanced CVD process and a PVD process.

32. (New) The process of claim 26, wherein each of the thin and thick tensile and compressive films are formed by deposition on an SiO_2 liner.

33. (New) The process of claim 26, wherein the process produces a tensile stress that enhances electron mobility in the nFETS without materially degrading performance of the pFETS and a compressive stress that enhances hole mobility in the pFETS without materially degrading performance of the nFETS.

CLAIM 34 (CANCELLED)

35. (New) The process of claim 26, wherein each of the thin and thick compressive films are formed before each of the thin and thick tensile films.

36. (New) The process of claim 26, wherein each of the thin and thick tensile films are formed before each of the thin and thick compressive films.

37. (New) The process of claim 26, wherein each of the thin compressive and tensile films are formed before each of the thick compressive and tensile films.

38. (New) The process of claim 26, wherein each of the thick compressive and tensile films are formed before each of the thin compressive and tensile films.